Multisupply Supervisor/Sequencer with Margining Control and Auxiliary ADC Inputs

Preliminary Technical Data

ADM1066

FEATURES

- 10 supply fault detectors enabling supervision of supplies to better than 1% accuracy
- 5 selectable input attenuators allow supervision:
  - Supplies up to 14.4 V on VH
  - Supplies up to 6 V on VP1-4
- 5 dual function inputs VX1-5:
  - High impedance input to supply fault detector with thresholds between 0.573 V and 1.375 V
  - General-purpose logic input
- Device powered by the highest of VP1–4, VH
- 2.048 V reference (±0.3%) on REFOUT pin
- 12-bit ADC for read-back of all supervised voltages
- Reference input, REFIN—2 input options:
  - Driven directly from REFOUT
  - More accurate external reference for improved ADC performance
- 6 voltage output 8-bit DACs (0.300 V to 1.551 V)
- 2 Auxiliary (single- ended) ADC inputs
- 10 programmable output drivers (PDO1-10)
  - Open collector with external pull-up
  - Push-pull output, driven to VDDCAP or VPn
  - Open collector with weak pull-up to VDDCAP or VPn
  - Internally charge pumped high drive for use with external N-FET (PDO1–6 only)
- Sequencing Engine (SE) implements State Machine control of PDO outputs:
  - State changes conditional on input events
  - Can enable complex control of boards
  - Power up and power down sequence control
  - Fault event handling
  - Interrupt generation on warnings
  - Watchdog function can be integrated in SE
  - Program software control of sequencing through SMBus
- User EEPROM: 256 Bytes
- Industry standard 2-wire bus interface (SMBus)
- Guaranteed PDO low with VH, VPn = 1.2 V
- 40-lead LFCSP and 48-lead TQFP packages

FUNCTIONAL BLOCK DIAGRAM

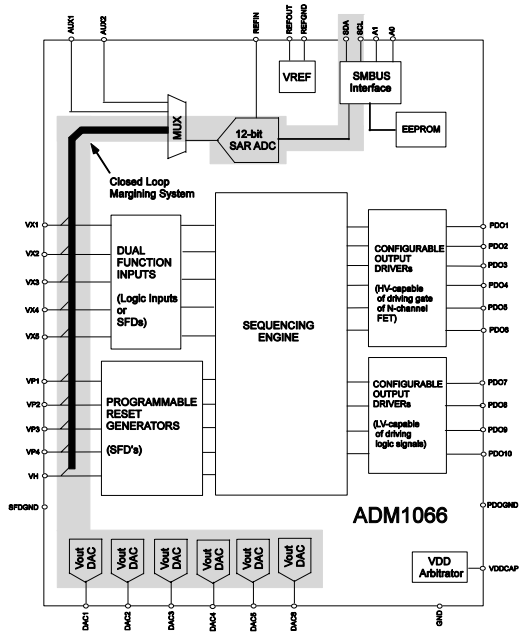

Figure 1.

APPLICATIONS

- Central office systems
- Servers/routers
- Multivoltage system line cards
- DSP/FPGA supply sequencing
- In circuit testing of margined supplies

GENERAL DESCRIPTION

The ADM1066 is a configurable supervisory/sequencing device which offers a single chip solution for supply monitoring and sequencing in multiple supply systems. In addition to these functions the ADM1066 integrates a 12-bit ADC and six 8-bit voltage output DACs. These circuits can be used to implement a closed loop margining system. This enables supply adjustment by altering either the feedback node or reference of a DC/DC Converter using the DAC outputs.

(continued on Page 3)

Rev. PrL

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

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REVISION HISTORY

Revision PrL: Update of specifications

Revision PrK: Preliminary Version

GENERAL DESCRIPTION

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The supply margining can be performed, with a minimum of external components. The margining loop can be used at In Circuit Testing of a board during production (to verify the board's functionality at say −5% of nominal supplies), or can be used dynamically to accurately control the output voltage of a DC/DC converter.

The device also provides up to ten programmable inputs for monitoring Under, Over, or out-of-window faults on up to ten supplies. In addition, ten programmable outputs are provided. These can be used as logic enables. Six of them can also provide up to a +12V output for driving the gate of an N- Channel FET which may be placed in the path of a supply.

The logical core of the device is a Sequencing Engine. This is a state machine based construction, providing up to 63 different states. This enables very flexible sequencing of the outputs, based on the condition of the inputs.

The device is controlled via configuration data which can programmed into an EEPROM. All of this configuration can be programmed using an intuitive GUI based software package provided by ADI.

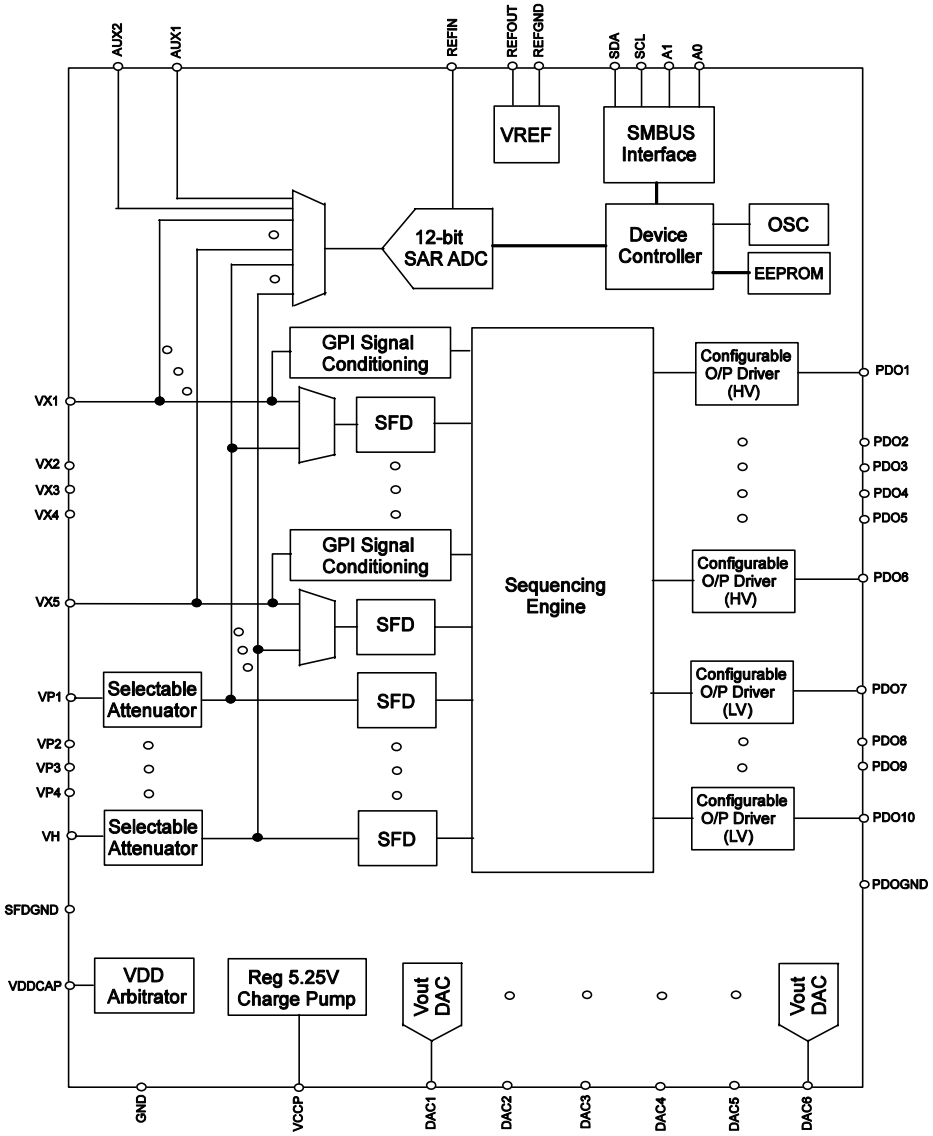

Figure 2. Detailed Block Diagram

ADM1066 SPECIFICATIONS[1]

VH = 3.0 V to 14.4 V, VPn = 3.0 V to 6.0 V[2], T_A = −40°C to 85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY ARBITRATION					
VH, VPn	3.0			V	Min. of VDDCAP=2.7V required
VP			6.0	V	Max VDDCAP= 5.1V, Typical
VH			14.4	V	VDDCAP = 4.75V
VDDCAP		4.75	5.4	V	Any VPn =6.0V, VH = 14.4V
POWER SUPPLY					
Supply Current, I_{VH}, I_{VPn} (DAC's, and ADC off)		3.5	8	mA	VDDCAP=4.75V, no PDO FET Drivers on, no loaded PDO pullups to VDDCAP
Additional Currents					
All PDO FET Drivers on		1		mA	VDDCAP=4.75V, (loaded with 1µA), no PDO pullups to VDDCAP.
Current available from VDDCAP			2	mA	Max. additional load that can be drawn from PDO pullups to VDDCAP
DAC's Supply Current		2		mA	6 DAC's on with 100µA max load on each
ADC Supply Current		1		mA	Running Round Robin loop
EEPROM Erase Current		10		mA	1ms duration only. VDDCAP=3V
SUPPLY FAULT DETECTORS					
VH Pin					
Input Impedance		22		kΩ	From VH to GND
Input attenuator error			±0.1	%	Mid range
			±0.2	%	High range
Detection Ranges					
High Range	6		14.4	V	
Mid Range	2.5		6	V	
VPn Pins					
Input Impedance		50		kΩ	From VPn to GND
Input attenuator error			±0.1	%	Low and Mid ranges
Detection Ranges					
Mid Range	2.5		6	V	
Low Range	1.25		3	V	
Ultra Low Range	0.573		1.375	V	No input attenuation error
VX Pins					
Input Impedance	1			MΩ	
Detection Ranges					
Ultra Low Range	0.573		1.375	V	No input attenuation error
Absolute Accuracy			±1	%	Input attenuator error + Vref Error + DAC Non Linearity + Comparator Offset Error
Threshold Resolution		8		bits	
Digital Glitch Filter	0		100	µs	8 filter length options
ANALOG TO DIGITAL CONVERTER					
Signal Range	0		V_{REFIN}	V	The ADC can convert signals presented to the VH, VPn and VX_GPIn pins.VPn and VH input signals are attenuated depending on selected range. A signal at the pin corresponding to the selected range will be between 0.573V and 1.375V at the ADC input.
Input reference voltage on REFIN pin, VREFIN		2.048	TBD	V	VDDCAP=2.7V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
			TBD	V	VDDCAP=4.75V
Resolution		12		bits	
INL			±2.5	lsb	End-point corrected, V_{REFIN}=2.048V
Gain Error			±0.05	%	V_{REFIN} = 2.048V
Offset Error			±2	lsb	V_{REFIN} = 2.048V
Input Noise		0.25		lsb_{rms}	Direct input (no attenuator)
BUFFERED VOLTAGE OUTPUT DACS					
Resolution		8		bits	
Code 80h output voltage					6 DAC's are individually selectable to be centered on one of four output voltage ranges
Range 1		0.6		V	
Range 2		0.8		V	
Range 3		1		V	
Range 4		1.25		V	
Mid code error			±6	mV	
Output voltage range		601.25		mV	Same range independent of centre point
lsb step size		2.36		mV	
INL			±1	lsb	End point corrected
DNL			±0.4	lsb	
Gain Error			1	%	
Max Load Current (source)			100	µA	
Max Load Current(sink)			100	µA	
Max load Capacitance			50	pF	
Settling time into 50pF load[3]			2	µs	
Load regulation		2.5		mV	per mA
PSRR		60		dB	DC
		40		dB	100mV step in 20ns with 50pF load
REFERENCE OUTPUT					
Reference Output Voltage	2.043	2.048	2.054	V	No Load
Max load current (source)			200	µA	
Max load current (sink)			100	µA	
Min load capacitance	100			nF	Cap required for decoupling, stability
Load regulation		2		mV	per 100µA
PSRR		60		dB	DC
PROGRAMMABLE DRIVER OUTPUTS					
High Voltage (Charge Pump) Mode (PDO1-6)					
Output Impedance		500		kΩ	
V_{OH}	11	12.5	14	V	I_{OH} =0
	10.5	12		V	I_{OH} =1µA
I_{outavg}		20		µA	2V < V_{OH}< 7V
Standard (Digital Output Mode (PDO1-10))					
V_{OH}[3]	2.4			V	V_{PU}(Pullup to VDDCAP or V_{PN}) = 2.7V, I_{OH} = 0.5mA
			4.75	V	V_{PU} to V_{pn} = 6.0V, I_{OH} = 0mA
	V_{PU}–0.3			V	V_{PU}< = 2.7V, I_{OH} = 0.5mA
V_{OL}	0		0.75	V	I_{OL} = 20mA
I_{OL}			20	mA	Max sink current per PDO pin
I_{SINK}			60	mA	Max total sink for all PDOs
R_{PULLUP}		20		kΩ	Internal pullup

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
I_{SOURCE}(VPn)			2	mA	Current Load on any VPn pull- ups (ie) total source current available through any number of PDO pull-up switches configured on to any one
Tristate Output Leakage Current			10	µA	V_{PDO}= 14.4V
Oscillator Frequency		100		KHz	All on- chip time delays derived from this clock
DIGITAL INPUTS (VXn,A0,A1)					
Input High Voltage, V_{IH}	2.0			V	Max. V_{IN}=5.5V
Input Low Voltage, V_{IL}			0.8	V	Max. V_{IN}=5.5V
Input High Current, I_{IH}	–1			µA	VIN= 5.5V
Input Low Current, I_{IL}			1	µA	VIN= 0
Input Capacitance		TBD		pF	
Programmable Pulldown Current, $I_{PULLDOWN}$		20		µA	VDDCAP=4.75. T_A=25^{0}CIf known logic state required
SERIAL BUS DIGITAL INPUTS (SDA,SCL)					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.8	V	
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = -3.0mA
SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}			400	KHz	
Bus Free Time, t_{BUF}	4.7			µs	
Start Setup Time, $t_{SU;STA}$	4.7			µs	
Start Hold Time, $t_{HD;STA}$	4			µs	
SCL Low Time, t_{LOW}	4.7			µs	
SCL High Time, t_{HIGH}	4			µs	
SCL, SDA Rise Time, t_r			1000	µs	
SCL, SDA Fall Time, t_f			300	µs	
Data Setup Time, $t_{SU;DAT}$	250			ns	
Data Hold Time, $t_{HD;DAT}$	300			ns	

[1] These are pre-release specifications and subject to change.
[2] At least one of the VH, VP1-4 pins must be ≥ 3.0V to maintain device supply on VDDCAP.
[3] Guaranteed by Characterization.
[4] Guaranteed by Design.

PIN CONFIGURATIONS AND FUNCTIONAL DESCRIPTIONS

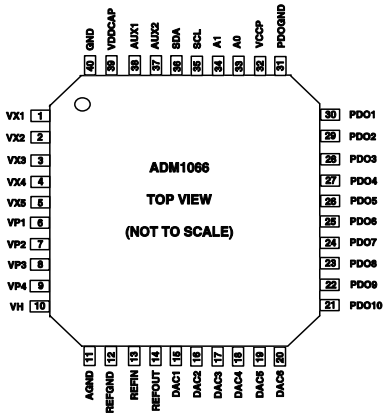

Figure 3. LFCSP Pin Configuration

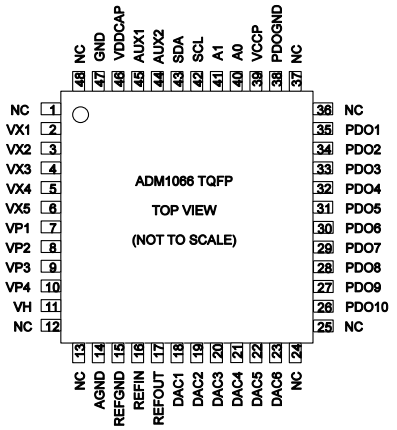

Figure 4. TQFP Pin Configuration

Table 2. Pin Functional Descriptions

Pin No.			
LFCSP	**TQFP**	**Mnemonic**	**Description**
	1	NC	No connection.
1–5	2-6	VX1–5	High impedance inputs to supply fault detectors. Fault thresholds can be set at between 0.573 V and 1.375 V. Alternatively these pins can be used as general purpose digital inputs.
6–9	7-10	VP1–4	Low voltage inputs to supply fault detectors. Three input ranges can be set by altering the input attenuation on a potential divider connected to these pins, the output of which connects to a supply fault detector; these allow thresholds between 2.5 V to 6V, 1.25 V to 3 V and 0.573 V to 1.375 V.
10	11	VH	High voltage input to supply fault detectors. Three input ranges can be set by altering the input attenuation on a potential divider connected to this pin, the output of which connects to a supply fault detector; these allow thresholds between 6V to 14.4V, 2.5 V to 6 V and 1.25 Vto 3 V.
	12-13	NC	No connection.
11	14	AGND	Ground return for input attenuators.
12	15	REFGND	Ground return for on-chip reference circuits.
13	16	REFIN	Reference input for ADC, nominally 2.048V.
14	17	REFOUT	2.048 V reference output.
15–20	18-23	DAC1–6	Voltage output DACs. Default to high impedance at power-up.
	24-25	NC	No connection.
21–30	26-35	PDO10–1	Programmable output drivers.
	36-37	NC	No connection.
31	38	PDOGND	Ground return for output drivers
32	39	VCCP	Central charge pump voltage of 5.25V. A reservoir capacitor must be connected between this pin and GND.
33	40	A0	Logic input which sets the seventh bit of the SMBus interface address.
34	41	A1	Logic input which sets the sixth bit of the SMBus interface address.
35	42	SCL	SMBus clock pin. Open drain output requiring external resistive pull-up.
36	43	SDA	SMBus data I/O pin. Open drain output requiring external resistive pull-up.
37	44	AUX2	Auxiliary, single ended, ADC Input
38	45	AUX1	Auxiliary, single ended, ADC Input
39	46	VDDCAP	Device supply voltage. Linearly regulated from the highest of the VP1-4,VH pins and clamped to a maximum of 4.75V
40	47	GND	Supply ground.
	48	NC	No connection.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Voltage on VH Pin	17 V
Voltage on VP Pins	7 V
Voltage on Any Other Input	−0.3 V to +6.5 V
Input Current at any pin	±5 mA
Package Input Current	±20 mA
Maximum Junction Temperature (T_{Jmax})	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering	
Vapor Phase, 60 s	215°C
ESD Rating all pins	2000 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

40-pin LFCSP Package:

θ_{JA} = TBD°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

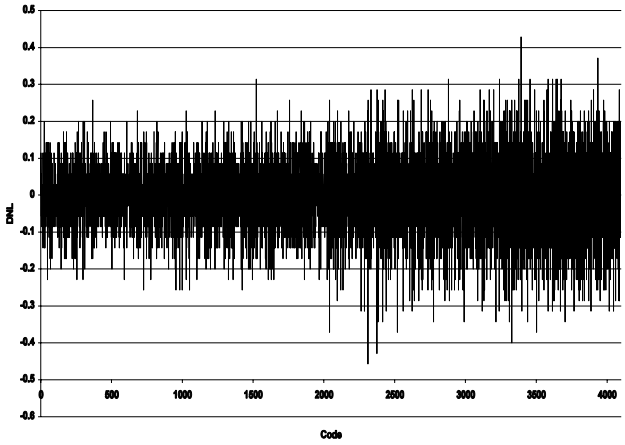

Figure 5. DNL for on- chip 12- bit ADC

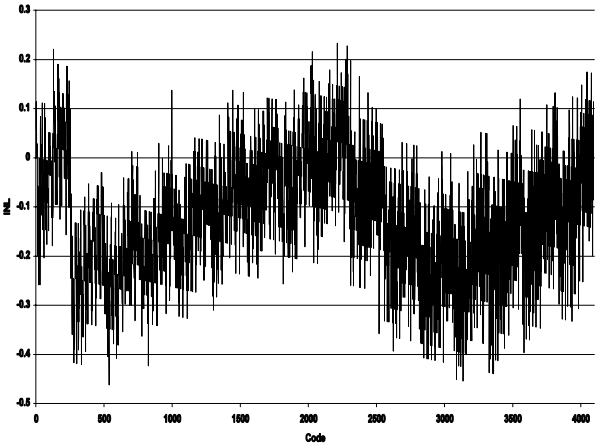

Figure 6. INL for on- chip 12- bit ADC

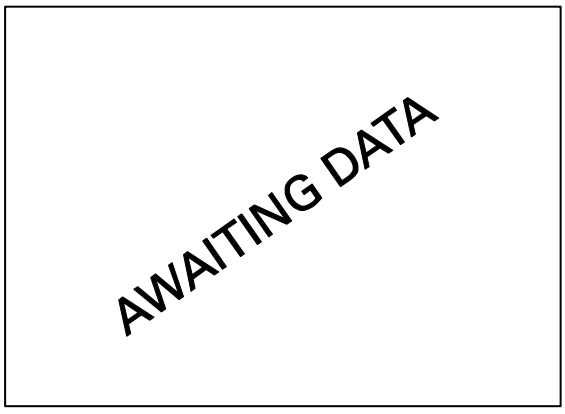

Figure 7. VVDDCAP vs. VVH and VVP1

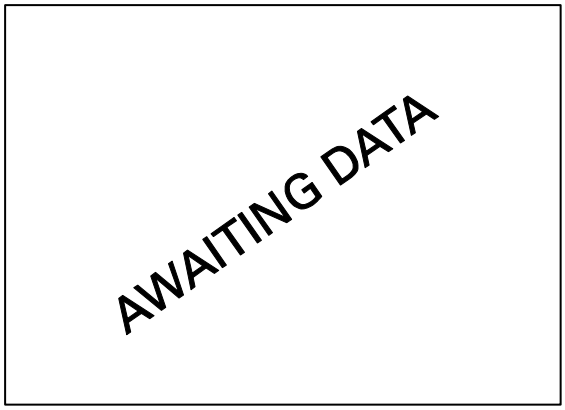

Figure 8. IDD vs. VVP1 (Supply)

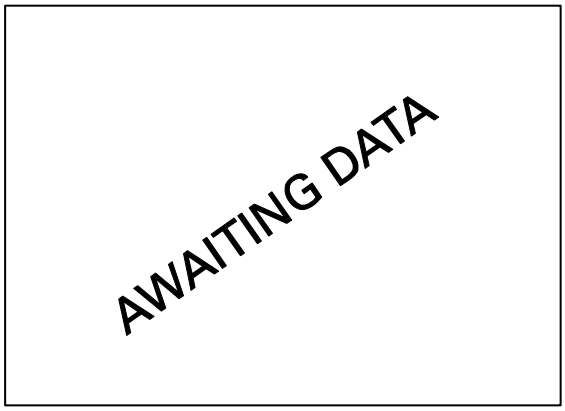

Figure 9. IVP1 vs. VVP1 (Not Supply)

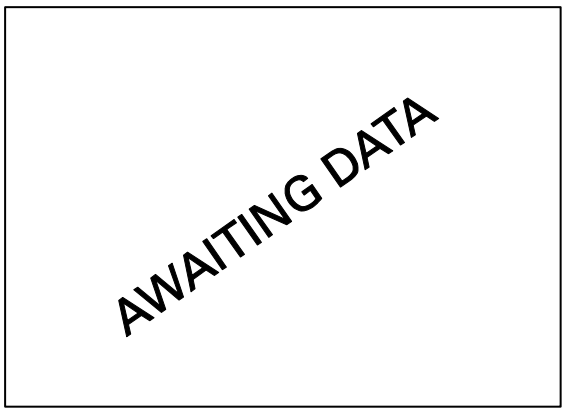

Figure 10. IDD vs. VVH

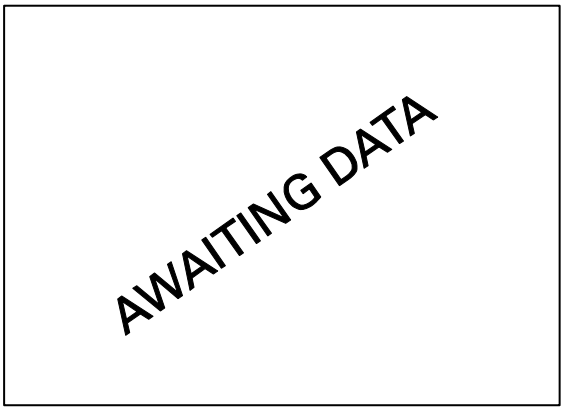

Figure 11. IVH vs. VVH (Not Supply)

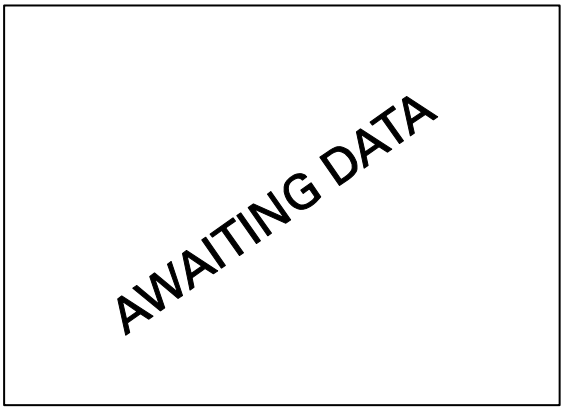

Figure 12. IVX1 vs. VVX1

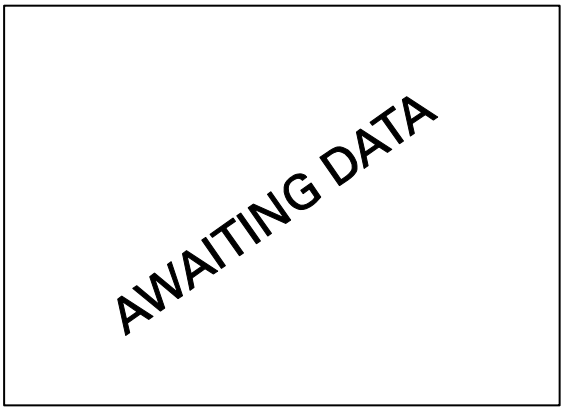

Figure 13. Percentage Deviation in VTHRESH vs. Temperature

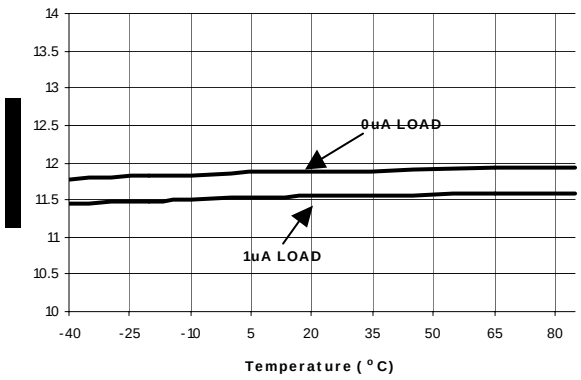

Figure 14. PDO Output (FET Drive Mode) vs. Temperature

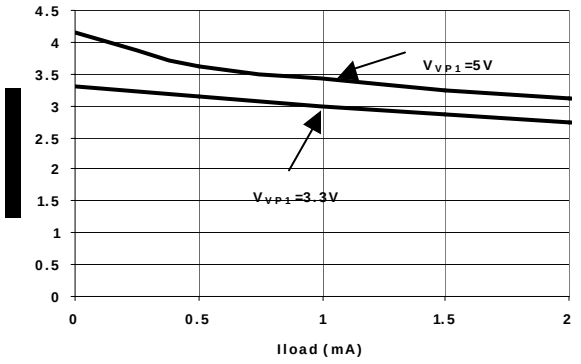

Figure 15. PDO Output (Strong Pull-up to VP1) vs. Load Curr.

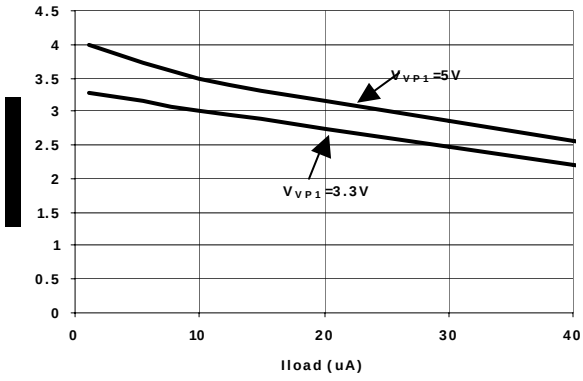

Figure 16. PDO Output (Weak Pull-up to VP1) vs. Load Current

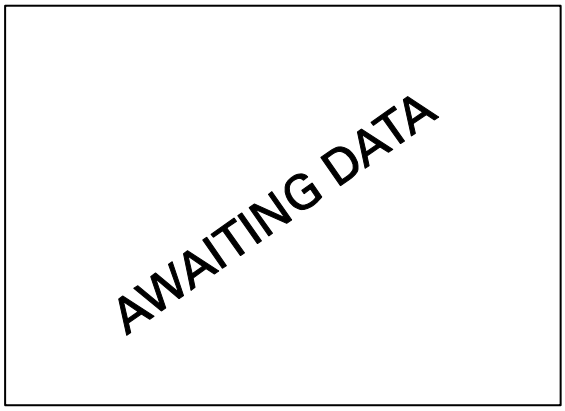

Figure 17. PDO Output (Strong Pull-Down) vs. Load Current

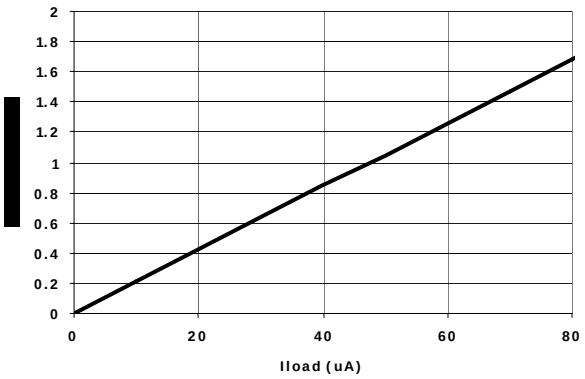

Figure 18. PDO Output (Weak Pull-Down) vs. Load Current

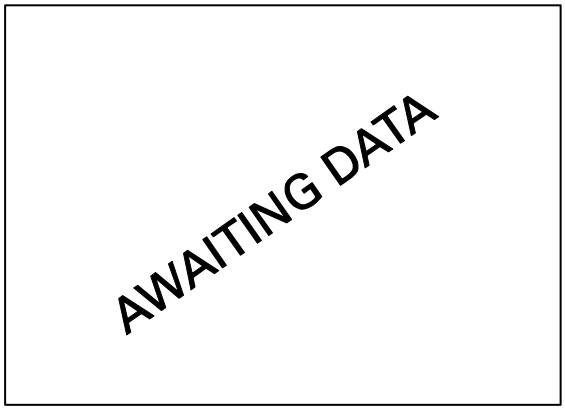

Figure 19. Oscillator Frequency vs. Temperature

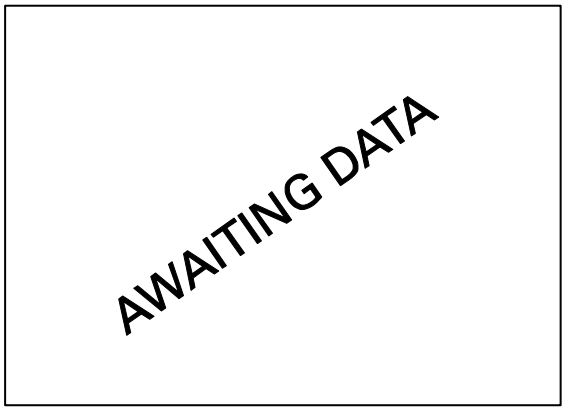

Figure 20. VCCP vs. Load Current

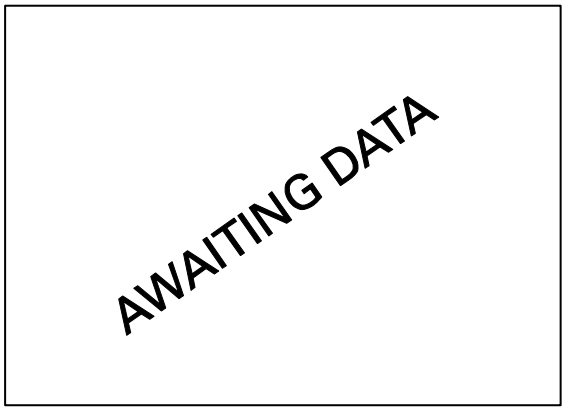

Figure 21. VXn (Digital Input Mode) Threshold vs. Temperature

ADM1066 INPUTS

POWERING THE ADM1066

The ADM1066 is powered from the highest voltage input on either the Positive Only supply inputs (VPn) or the High Voltage supply input (VH). The same pins are used for supply fault detection (discussed below) . A V_{DD} Arbitrator on the device chooses which supply to use. The arbitrator can be considered an OR'ing of five LDO's together. A supply comparator chooses which of the inputs is highest and selects this one to provide the on- chip supply. There is minimal switching loss with this architecture (~0.2V), resulting in the ability to power the ADM1066 from a supply as low as 3.0V. Note that the supply on the VXn pins cannot be used to power the device.

An external cap to GND is required to decouple the on chip supply from noise. This cap should be connected to the VDDCAP pin, as shown in Figure 22. The cap has another use during "brown outs" (momentary loss of power). Under these conditions, where the input supply, VPn or VH, dips transiently below V_{DD}, the synchronous rectifier switch immediately turns off so that it doesn't pull V_{DD} down. The V_{DD} cap can then act like a reservoir and keep the device active until the next highest supply takes over the powering of the device. 10µF is recommended for this reservoir/decoupling function.

Note that in the case where there are two or more supplies within 100mV of each other, the supply which takes control of V_{DD} first will keep control (e.g) if VP1 is connected to a 3.3V supply, then V_{DD} will power up to approximately 3.1V through VP1. If VP2 is then connected to another 3.3V supply, VP1 will still power the device, unless VP2 goes 100mV higher than VP1.

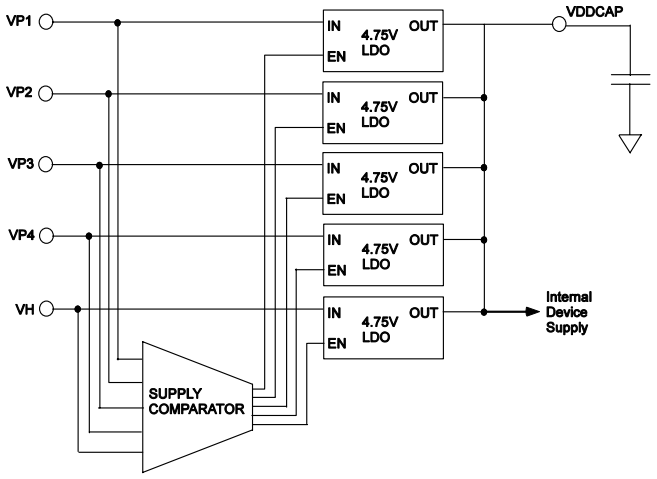

Figure 22. VDD Arbitrator Operation

The ADM1066 has ten programmable inputs. Five of these are dedicated Supply Fault Detectors (SFD's). These dedicated inputs are called VH and VP1-4 by default. The other five inputs have dual functionality. They can either be used as Supply Fault Detectors, with similar functionality to VH and VP1-4, or they can be used as CMOS/TTL compatible logic inputs to the devices. Thus, the ADM1066 can have up to ten analog inputs, a minimum of five analog inputs and five digital inputs, or a mix. Note that if an input is used as an analog input, it cannot be used as a digital input. Thus, a configuration requiring ten analog inputs would have no digital inputs available. Table 4 shows the details of each of the inputs.

Table 4. Input Functions, Thresholds and Ranges

Input	Function	Voltage Range	Max Hysteresis	Voltage Resolution	Glitch Filter
VH	High V Analog Input	2.5V to 6V	425mV	13.7mV	0-100µs
		4.8V to 14.4V	1.16V	37.6mV	0-100µs
VPn	Positive Analog Input	0.573 to 1.375V	97.5mV	3.14mV	0-100µs
		1.25 to 3V	212mV	6.8mV	0-100µs
		2.5 to 6V	425mV	13.7mV	0-100µs
VXn	High Z Analog Input	0.573 to 1.375V	97.5mV	3.14mV	0-100µs
	Digital Input	0 to 5V	N/A	N/A	0-100µs

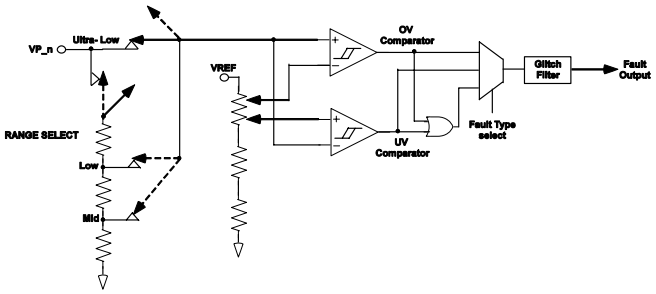

Figure 23. Supply Fault Detector Block

SUPPLY SUPERVISION

The ADM1066 has up to ten Supply Fault Detectors (SFDs) on its ten input channels. These are highly programmable reset generators. This enables the supervision of up to ten supply voltages. These supplies can be as low as 0.573V and as high as 14.4V. The inputs can be configured to detect an Undervoltage fault (where the input voltage droops below a preprogrammed value), an Overvoltage fault (where the input voltage rises above a preprogrammed value) or an Out-Of-Window fault (undervoltage OR overvoltage). The thresholds can be programmed to 8-bit resolution in registers provided in the ADM1066. This translates into a voltage resolution which is dependent on the range selected. The

resolution is given by

$$Step\ Size = Theshold\ Rang / 255$$

Thus, if the high range were selected on VH, the UV and

$$(14.4V - 4.8V) / 255 = 37.6mV$$

Listed below are the upper and lower limit of each range available, the bottom of each range and the range itself. The threshold value required is given by

$$V_T = (V_{R^X} N) / 255 + V_B$$

Table 5.

Voltage Range	V_B(V)	V_R(V)
0.573 to 1.375V	0.573	0.802
1.25 to 3V	1.25	1.75
2.5 to 6V	2.5	3.5
4.8 to 14.4V	4.8	9.6

where:

V_T is the desired threshold voltage (UV or OV).
V_R is the voltage range.
N is the decimal value of the 8-bit code.
V_B is the bottom of the range.

Reversing the equation, the code for a desired threshold is given by

$$N = 255 \times (V_T - V_B) / V_R$$

For example, if the user wishes to set a 5V OV threshold on VP1, the code to be programmed in the PS1OVTH register (discussed in AN-698) would be

$$N = 255 \times (5 - 2.5) / 3.5$$

$$Thus\ N = 182\ (10110110\ Bin, or\ 0xB6)$$

INPUT COMPARATOR HYSTERESIS

The UV and OV comparators shown in Figure 22 are always looking at VPn. In order to avoid chattering (multiple transitions when the input is very close to the set threshold level), these comparators have digitally programmable hysteresis. The hysteresis can be programmed up to the values shown in Table 4. The hysteresis is added after a supply voltage goes out of tolerance. Thus, the user can program how much above the UV threshold the input must rise again before a UV fault is de-asserted. Similarly, the user can program how much below the OV threshold an input must fall again before an OV fault is de-asserted.

The hysteresis figure is given by

$$V_{HYST} = V_R \times N_{THREST} / 255$$

where:

V_{HYST} is the desired hysteresis voltage.
N_{THRESH} is the decimal value of the 5 bit hysteresis code.

Note that N_{THRESH} has a maximum value of 31. The maximum hysteresis for each of the ranges is quoted in Table 4.

INPUT GLITCH FILTERING

The final stage of the SFD's is a glitch filter. This block provides time domain filtering on the output of the SFD comparators. This allows the user to remove any spurious transitions (such as supply bounce at turn-on). The glitch filter function is additional to the digitally programmable hysteresis of the SFD comparators. The glitch filter timeout is programmable up to 100µs. The functionality of the block is best explained using an example. A glitch filter timeout of 100µs means that pulses which appear on the input of the glitch filter block and are less than 100_s in duration will be prevented from appearing on the output of the glitch filter block. Any input pulse which is longer in duration than 100µs will appear on the output of the glitch filter block. The output will be delayed with respect to the input by 100µs. The filtering process is shown in Figure 24.

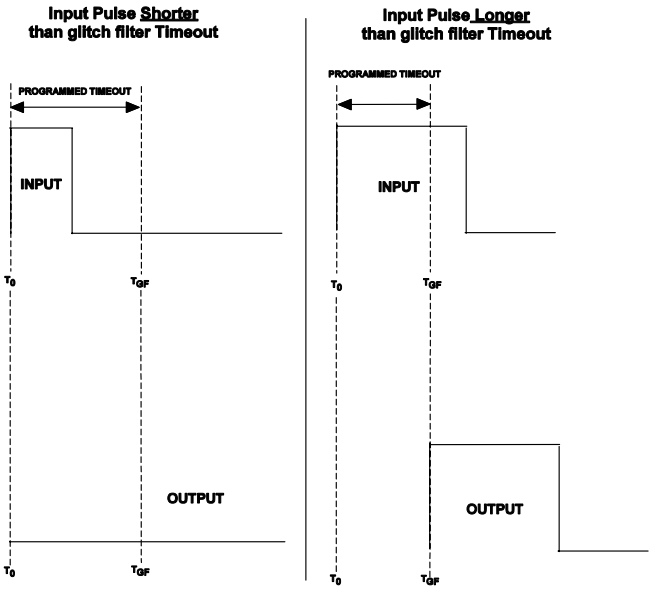

Figure 24. Input Glitch Filter Function

SUPPLY SUPERVISION WITH VXN INPUTS

The VXn inputs have two functions. They can either be used as Supply Fault Detectors or as digital logic inputs. When selected to be an analog (SFD) input, the VXn pins have very similar functionality to the VH and VPn pins. The major difference is that the VXn pins have only one input range, 0.573V to 1.375V. Therefore, these inputs can only supervise very low supplies directly. However, the input impedance of the VXn pins is high, allowing an external resistor divide network to be connected to the pin. Thus, any supply can be potentially divided down into the input range of the VXn pin and supervised. This enables other supplies such as +24V, +48V, −5V to be monitored by the ADM1066.

An additional Supply Supervision function is available when the VXn pins are selected as digital inputs. In this case, the analog function is available to be used as a second detector on each of the dedicated analog inputs, VP1-4 and VH. THe analog function of VX1 is mapped to VP1, VX2 is mapped to VP2 etc. VX5 is mapped to VH. In this case, these SFD's can be viewed as a secondary or "Warning" SFD. These secondary SFD's are fixed to the same input range as the primary SFD. They are used to indicate Warning levels rather than Failure levels. This allows faults and warnings to be generated on a single supply using only one pin. For example, if VP1 was set to output a fault if a 3.3V supply drooped to 3.0V, VX1 could be set to output a warning at 3.1V. Warning outputs are available for readback from the status registers. They are also OR'ed together and fed into the Sequencing Engine (SE), allowing Warnings to generate interrupts on the PDO's. Thus, in the example above, if the supply drooped to 3.1V, a warning would be generated, and remedial action could be taken before the supply dropped out of tolerance.

SUPPLY SUPERVISION USING THE ADC

A further level of supervision is provided by the on- chip 12 bit ADC. The ADC has a twelve channel analog mux on the front end. The twelve channels are the ten SFD inputs and two auxiliary (single ended) ADC inputs. Any or all of these inputs can be selected to be read in turn by the ADC. The circuit controlling this operation is called the "Round Robin". The Round Robin can be selected to run through its loop of conversions just once or continuously. Averaging is also provided for each channel. In this case the Round Robin will run through its loop of conversions sixteen times before returning a result for each channel. At the end of this cycle the results are all written to the output registers.
Limit registers are provided on the ADM1066 which the user can program to a maximum or minimum allowable threshold. Exceeding the threshold generates a Warning which can be read back from the status registers or inputted into the SE to determine what sequencing action the ADM1066 should take. Only one register is provided for each input channel so an UV or OV threshold but not both can be set for a given channel. The round robin can be enabled either via an SMBus write, or can be programmed to turn on in any state in the SE program, for instance it can be set to start once a powerup sequence is complete and all supplies are known to be within expected tolerance limits. Note that there is a latency built into this supervision which is dictated by the conversion time of the ADC. With all twelve channels selected the total time for the round robin operation (averaging off) will be approximately 6ms (500µs per channel selected). Supervision using the ADC, therefore, does not provide the same real time response as the SFD's.

The ADC samples single-sided inputs with respect to the AGND pin. A 0V input gives out code 0 and an input equal to the voltage on REFIN gives out full code (4095 (dec))

The inputs to the ADC come directly from the VXn pins and from the back of the input attenuators on the VPn and VH pins, as shown in Figure 25 and 26 below.

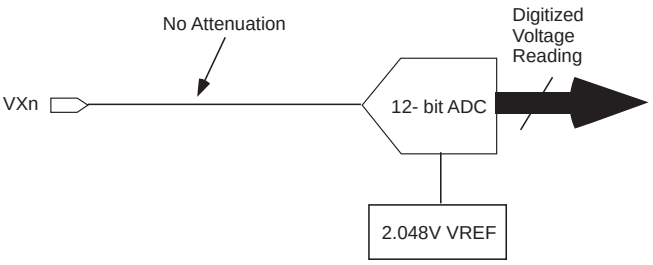

Figure 25. ADC Reading on VXn pins

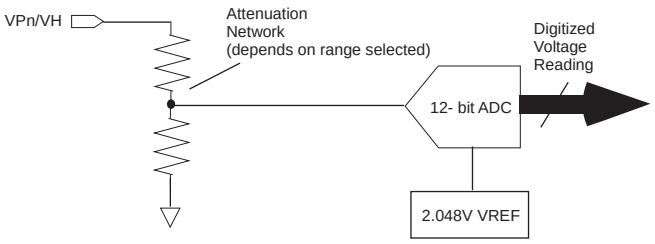

Figure 26. ADC Reading on VXn pins

The voltage at the input pin can be derived from the following equations:-

$$V = \frac{ADCcode}{4095} \times AttenuationFactor \times 2.048V$$

The ADC input voltage range for each of the SFD input ranges is given in table 6 below.

Table 6.

SFD Input Range	Attenuation Factor	ADC Input voltage range
0.573 to 1.375V	1	0 to 2.048V
1.25 to 3V	2.181	0 to 4.46V
2.5 to 6V	4.363	0 to 6.0V*
4.8 to 14.4V	10.472	0 to 14.4V*

* The upper limit is the absolute maximum allowed voltage on these pins.

It is normal to supply the reference to the ADC on the REFIN pin simply by connecting the REFOUT pin to the REFIN pin. REFOUT provides a 2.048V reference. As such, the supervising range covers less that half of the normal ADC range. It is possible to provide the ADC with a more accurate external reference for improved read-back accuracy.

Also, it is possible to connect supplies to the input pins purely for ADC read-back even though they may go above the expected supervisory range limits (though not above 6V as this would violate the absolute maximum ratings on these pins). For instance a 1.5V supply connected to the VX1 pin would correctly read out as an ADC code of approximately 3/4 Full scale but would always sit above any supervisory limits that could be set on that pin.

It is not possible to set REFIN to higher than 2.048V.

VXN PINS AS DIGITAL INPUTS

As outlined previously, the VXn inputs pins on the ADM1066 have dual functionality. The second function is as a digital input to the device. Thus, the ADM1066 can be configured to have up to five digital inputs. These inputs are TTL/CMOS compatible. Standard logic signals can be applied to the pins: RESET from reset generators, PWRGOOD signals, fault flags, manual resets, and so on. These signals are available as inputs to the SE, and so can be used to control the status of the PDO's. The inputs can be configured to detect either a change in level or an edge. When configured for level detect, the output of the digital block is simply a buffered version of the input. When configured for edge detect, once the logic transition is detected, a pulse of programmable width is outputted from the digital block. The width is programmable from 0µs to a maximum of 100µs. The digital blocks feature the same glitch filter function available on the SFD's. This enables the user to ignore spurious transitions on the inputs. For example, the filter can be used to debounce a manual reset switch. When configured as digital inputs, each of the VXn pins has a weak (10µA) pull-down current source available for placing the input in a known condition, even if left floating. The current source, if selected, weakly pulls the input to GND.

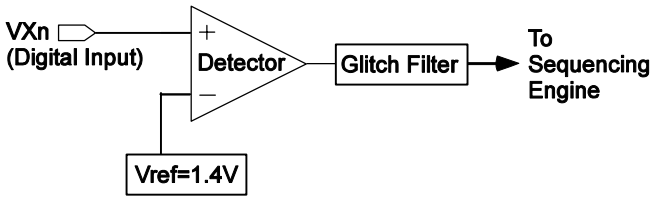

Figure 27. VXn Digital Input Function

ADM1066 OUTPUTS

SUPPLY SEQUENCING THROUGH CONFIGURABLE OUTPUT DRIVERS

Supply sequencing is achieved with the ADM1066 by using the Programmable Driver Outputs (PDO's) on the device as control signals for supplies. The Output drivers can either be used as logic enables or as FET drivers.

The sequence in which the PDO's are asserted (and, thus, the supplies are turned on) is controlled by the Sequencing Engine (SE). The SE determines what action is to be taken with the PDO's based on the condition of the inputs of the ADM1066. Thus, the PDO's can be set up to assert when the SFD's are in tolerance, the correct input signals are received on the VXn digital pins, there are no warnings from any of the inputs of the device, and so on. The PDO's can be used for a number of functions: the primary function is to provide Enable signals for LDO's or DC/DC convertors which generate supplies locally on a board. The PDO's can also be used to provide a POWER_GOOD signal when all of the SFD's are in tolerance or provide a RESET output if one of the SFD's goes out of spec (this can be used as a status signal for a DSP, FPGA or other microcontroller).

The PDO's can be programmed to pull- up to a number of different options. The outputs can be programmed as:–

- Open Drain (allowing the user to connect an external pull-up resistor)
- Open Drain with weak pull-up to VDD
- Push Pull to VDD
- Open-drain with weak pull-up to VPn
- Push-pull to VPn
- Strong pull-down to GND
- Internally charge- pumped high drive (12V- PDO 1- 6 Only)

The last option (available only on PDO's 1 to 6) allows the user to directly drive a voltage high enough to fully enhance an external N-fet which is used to isolate, for example, a card-side voltage from a backplane supply (a PDO will sustain greater than 10.5V into a 1µA load). The pull-down switches may be used to drive status LEDs.

The data driving each of the PDO's can come from one of three sources. The source can be enabled in the PnPDOCFG configuration register (refer to AN-698).
The data sources are:

- An output from the SE.
- Directly from the SMBus. A PDO can be configured so that the SMBus has direct control over it. This enables software control of the PDO's. Thus, a microcontroller could be used to initiate a software power-up/power-down sequence.
- An On- Chip Clock. A 100KHz clock is generated on the device. This clock can be made available on any of the PDO's. It could be used to clock an external device such as a LED, for example.

The default condition of the PDO's is to be pulled to GND by a weak (20kΩ) on-chip pull-down resistor. This is also the condition of the PDO's on power-up until the configuration is downloaded from EEPROM and the programmed setup is latched. The outputs are actively pulled low once there is a supply 1V or greater on VPn or VH. The outputs remain high impedance prior to 1V appearing on VPn or VH. This provides a known condition for the PDO's during power-up. The internal pull-down can be overdriven with an external pull-up of suitable value tied from the PDO pin to the required pullup voltage. The 20kΩ resistor must be accounted for in calculating a suitable value. For example, if it was required to pull PDOn up to 3.3V, and 5V was available as an external supply, the pull-up resistor value is given by:-

$$3.3V = 5V \times 20k\Omega / \left(R_{UP} + 20k\Omega\right)$$

Therefore,

$$R_{UP} = \left(100k\Omega - 66k\Omega\right) / 3.3 = 10k\Omega$$

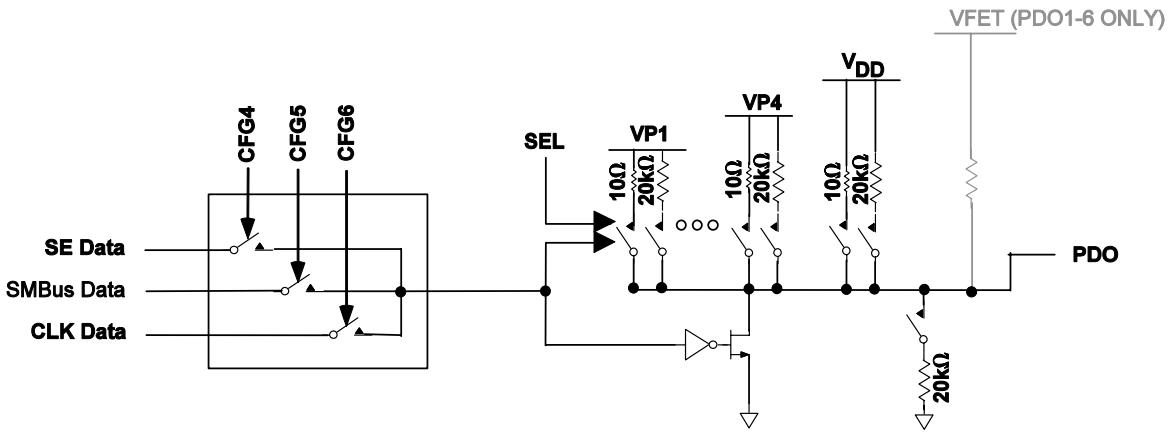

Figure 28. Programmable Driver Output

ADM1066 SEQUENCING ENGINE

The ADM1066 incorporates a Sequencing Engine (SE) which provides the user with powerful and flexible control of sequencing. The SE implements a state machine control of the PDO outputs, with state changes conditional on input events. SE programs can enable complex control of boards, such as powerup and power down sequence control, fault event handling, interrupt generation on warnings etc. A watchdog function, to verify the continued operation of a processor clock, can be integrated into the SE program. The SE can also be controlled via the SMBus, giving software or firmware control of the board sequencing

Considering the function of the SE from an applications viewpoint it is most instructive to think of the SE as providing a "state" for a state machine. This state has the following attributes:

- it is used to monitor signals indicating the status of the 10 input pins, VP1-4, VH and VX1-VX5
- it can be entered from any other state
- there are three exit routes which move the state machine on to a "next state", these are:
    1. End of Step detection
    2. Monitoring fault
    3. Timeout
- delay timers for the End of Step and Timeout blocks above can be programmed independently and will change with each state change. The range of timeouts is from 0ms to 400ms
- the output condition of the 10 PDO pins is defined and fixed within a state
- the transition from one state to the next is made in less than 20µs. This is the time taken to download a state definition from EEPROM to the SE.

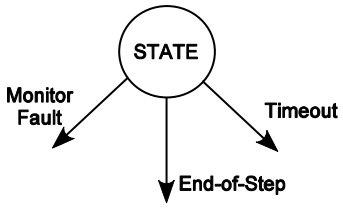

Figure 29. State Cell

The ADM1066 offers up to 63 such state definitions. The signals being monitored to indicate the status of the input pins are the outputs of the SFD's.

WARNINGS

The SE is also monitoring the Warnings. These are generated by ADC readings violating their limit register value or by the secondary voltage monitors on VP1-4, VH. These are all OR'ed together and available as a single "Warnings" input to each of the three blocks which enable exiting from a state.

SW FLOW-UNCONDITIONAL JUMP

The SE can be forced to advance to the next state unconditionally. This enables the user to force the SE to advance. Examples where this might be used include moving to a margining state or as a method of debugging a sequence. The SW Flow or Go to command can be seen as another input to End of Step and Timeout blocks which provide an exit from each state.

Table 6. Example Sequence States Entries

State	End of Step	Timeout	Monitor
IDLE1	If VX1 is LOW then go to State IDLE2		
IDLE2	If VP1 is OK then go to State EN3V3		
EN3V3	If VP2 is OK then go to State EN2V5	If VP2 is NOT OK after 10ms then goto State DIS3V3	If VP1 is NOT OK then goto State IDLE1
DIS3V3	If VX1 is HIGH then go to State IDLE1		
EN2V5	If VP3 is OK then go to State PWRGD	If VP3 is NOT OK after 20ms then goto State DIS2V5	If VP1 OR VP2 is NOT OK then goto State FSEL2
DIS2V5	If VX1 is HIGH the go to State IDLE1		
FSEL1	If VP3 is NOT OK then go to State DIS2V5		If VP1 OR VP2 is NOT OK then goto State FSEL2
FSEL2	If VP2 is NOT OK then go to State DIS3V3		If VP1 is NOT OK then goto State IDLE1
PWRGD	If VX1 is HIGH then go to State DIS2V5		If VP1 OR VP2 OR VP3 is NOT OK then goto State FSEL1

SEQUENCING ENGINE APPLICATION EXAMPLE

An example application will be considered here to demonstrate the operation of the SE. Figure 28 below shows how the simple building block of a single SE state can be used to build up a power-up sequence for a 3–supply system. Table 6 below textually describes the same SE implementation. In this system the presence of a "good" 5V supply on VP1, and the VX1 pin being held low, are the trigger required for an up sequence to start. The sequence intends to turn on the 3.3V supply next, then the 2.5V supply (assuming successful turn-on of the 3.3V supply). Once all 3 supplies are good the PWRGD state is entered, where the SE will remain until a fault occurs on one of the 3 supplies, or it is instructed to go through a power-down sequence by VX1 going high.

Faults are dealt with on the way through the up sequence on a case-by case basis. The text below which describes the individual blocks will use the example application to demonstrate what the state machine is doing.

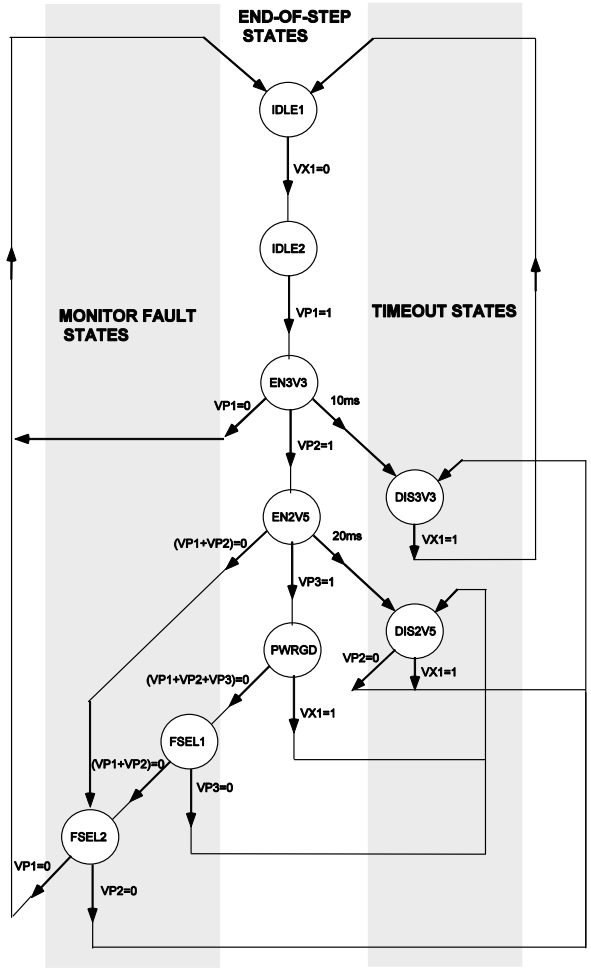

Figure 30. Flow Diagram

PDO Outputs	IDLE1	IDLE2	EN3V3	EN2V5	DIS3V3	DIS2V5	PWRGD	FSEL1	FSEL2
PDO1=3V3ON	0	0	1	1	0	1	1	1	1
PDO2=2V5ON	0	0	0	1	1	0	1	1	1
PDO3=FAULT	0	0	0	0	1	1	0	1	1

Figure 31. PDO outputs for each state

END OF STEP DETECTOR

This block is used to detect when a step in a sequence has been completed. It is simply looking for one of the inputs to SE to change state and is most often used to be the gate on successful progress through an up or down sequence. A timer block is included, in this detector- it can be thought of as a way to insert delays into an up or down sequence, if required. Timer delays can be set from 10µs to 400ms. Figure 32 shows a block diagram of the End of Step Detector.

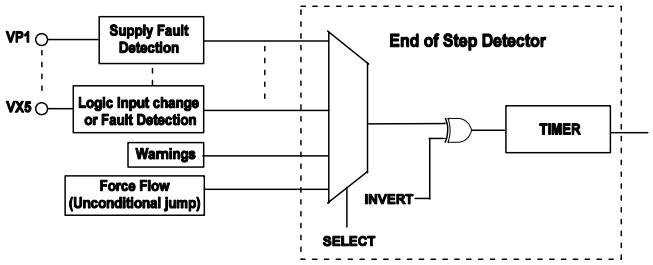

Figure 32. End-of-Step Detector

It is also possible to use the End of Step Detector to help identify monitoring faults. In the example application shown in Figure 30 it can be seen how the FSEL1 and FSEL2 states are being used to identify which of VP1,VP2 or VP3 has faulted and to take the appropriate action.

MONITORING FAULT DETECTOR

This block is used to detect a failure on any one of a number of inputs. The logical function implementing this is a wide OR gate which is used to detect when any one of a number of inputs deviates from its' expected condition. The clearest demonstration of the use of this block is in the PWRGD state where the monitor block will indicate that a failure on any one of the VP1,VP2 and VP3 inputs has occurred. There is no programmable delay available in this block. This is because, the triggering of a fault condition is likely to be caused by a supply falling out of tolerance, a situation to which the user will want to react to as quickly as possible. There is some latency in moving out of this state, however, since it takes a finite time (~20µs) for the state configuration to download from EEPROM into the SE. Figure 33 below shows a block diagram of the Monitoring Fault Detector.

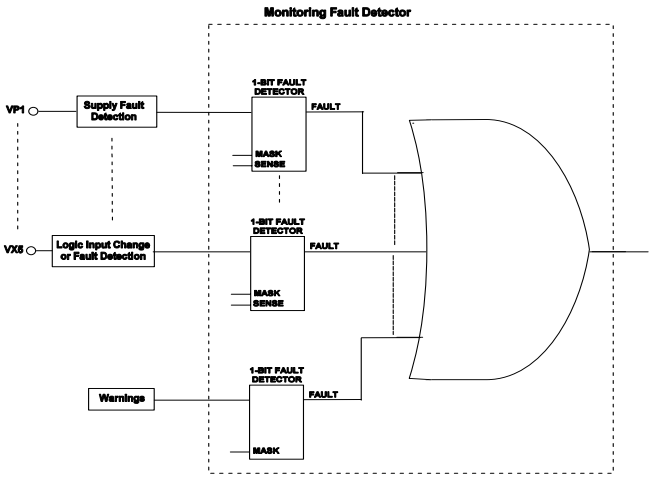

Figure 33. Monitoring Fault Detector

TIMEOUT DETECTOR

This block is included to allow the user to trap a failure to make proper progress through an up or down sequence.

In the example application we can see the timeout next state transition being used from the EN3V3 and EN2V5 states. In the case of the EN3V3 state, the signal 3V3ON is asserted on entry to this state (on the PDO1 output pin) to turn on a 3.3V supply. This supply rail is connected to the VP2 pin and the End of Step detector is looking for the VP2 to go "good" (going above its' UV threshold, which will be set on the Supply Fault Detector (SFD) attached to that pin). Progress forward in the up sequence is made when this change is detected.

If, however, the supply failed to go "good" – perhaps because of a short circuit over-loading this supply – then the timeout block allows this problem to be trapped. In the example shown, if the 3.3V supply does not go good within 10ms then the SE moves to the DIS3V3 state and turns off this supply by bringing PDO1 low. It also indicates that a fault has occurred by taking PDO3 high. Timeout delays of between 0µs and 400ms can be programmed.

CLOSED LOOP SUPPLY MARGINING

It is often necessary for the system designer to be able to adjust supplies, either to optimize their level, or to force them away from nominal values to characterize the system performance under these conditions. This is a function typically performed at In- Circuit Test (ICT), for instance, where the manufacturer wishes to guarantee that the product under test functions correctly at, say, nominal supplies –10%. The ADM1066 incorporates all the circuits required to do this, with a 12-bit successive approximation ADC to read back the level of any of the supervised voltages, and six voltage output DACs (DAC1–DAC6) which can be used to adjust supply levels. These circuits can be used along with some other "intelligence" such as a microcontroller to implement a closed loop margining system which will allow any dc-dc supply to be set to any voltage, accurate to within ±0.5% of the target.

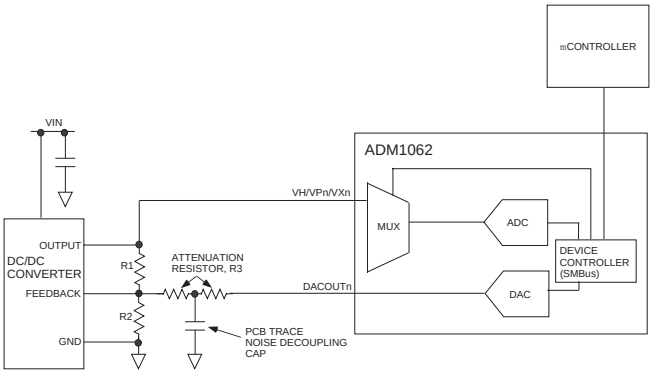

Figure 34. Closed Loop Margining System using ADM1066

The simplest circuit to implement this function is an attenuation resistor to connect the DACn pin to the feedback node of a dc-dc converter. When the DACn output voltage is set equal to the feedback voltage, no current is flowing in the attenuation resistor and the dc-dc output voltage will not change. Taking DACn above the feedback voltage forces current into the feedback node and the output of the dc-dc converter will be forced to fall to compensate for this. The dc-dc output can be forced high by setting the DACn output voltage lower than the feedback node voltage. The series resistor can be split in two and the node between them decoupled with a capacitor to ground. This will help to decouple any noise picked up from the board. Decoupling to a ground local to the dc-dc converter is recommended.

Then the simplest algorithm to implement closed loop margining is as follows:

1. Disable the six DACn outputs.
2. Set DAC output voltage equal to the voltage on the feedback node.
3. Enable the DAC.
4. Read the voltage at the dc-dc output (which will be connected to one of the VP1–4,VH or VX1–5 pins).
5. If necessary, modify the DACn output code up or down to adjust the dc-dc output voltage, otherwise, stop since target voltage has been reached.
6. Set the DAC output voltage to a value which alters the supply output by the required amount (eg) ±5%.
7. Repeat from 4.

Steps 1-3 ensure that when the DACn output buffer is turned on it has very little effect on the dc-dc output. The dac output buffer has been designed to power up without glitching. It does this by first powering up the buffer to follow the pin voltage and

does not drive out on to the pin at this time. Once the output buffer is properly enabled, the buffer input is switched over to the dac, and the output stage of the buffer is turned on. Output glitching is negligible.

WRITING TO THE DACs

Four DAC ranges are offered and these are placed with mid-code (code 0x7F) at 0.6V, 0.8V, 1.0V and 1.25V. These voltages are placed to correspond to the most common feedback voltages. Centering the dac outputs in this way provides the best use of the dac resolution i.e. for most supplies it will be possible to place the dac mid-code at the point where the dc-dc output is not modified, thus giving a full half of the dac range to margin up and and the other half to margin down. The dac output voltage is set by the code written to the DACn register. The voltage is linear with the unsigned binary number in this register. The code 0x7F is placed at the mid-code voltage as described above. The output voltage is given by the following equation:

$$Dac\ output = \left(DACn - 0x7F\right)/255 * 0.6015 + V_{OFF}$$

where V_{OFF} is one of the four "offset voltages" described above.

CHOOSING THE SIZE OF THE ATTENUATION RESISTOR

The full output swing of the DAC's is +/-300mV around whichever of the four mid code voltages is selected. The voltage range for each midcode voltage is shown in table X below.

Table 6. Margining DAC's- midcode, max and min voltages

Mid code Voltage	Minimum Voltage Output	Maximum Voltage Output
0.6V	0.3V	0.9V
0.8V	0.5V	1.1V
1.0V	0.7V	1.3V
1.25V	0.95V	1.55V

How much this DAC voltage swing affects the output voltage of the dc/dc converter being margined is determined by the size of the attenuation resistor, R3 (see figure 34).

Since the voltage at the feedback pin remains constant, , the current flowing from the feedback node to GND via R2 is a constant. Also, the feedback node itself is high impedance. This means that the current flowing through R1 is the same as the current flowing through R3. Therefore, there is a direct relationship between the extra voltage drop across R1 during margining and the voltage drop across R3. This relationship is given by the equation

$$\partial V_{OUT} = \frac{R1}{R3}\left(V_{FB} - V_{DACOUT}\right)$$

where,

∂V_{OUT} = the change in V_{OUT}

` V_{FB} = the voltage at the feedback node of the DC/DC Converter

V_{DACOUT} = the voltage output of the margining DAC

From this equation it can be seen that if the user wishes for the output voltage to change by +/-300mV, then R1=R3. If the user wishes for the output voltage to change by +/-600mV then R1=2xR3 etc.

It is best to use the full dac output range to margin a supply. Choosing the attenuation resistor in this way provides the most resolution out of the dac – in other words, with one dac code change the smallest effect on the dc-dc output voltage is induced. If the resistor is sized up to use code,say , 27(dec) to 227(dec) to move the dc-dc output by ±5%, then that is 100 codes to move 5% i.e. each code moves the output by 0.05%. This is beyond the readback accuracy of the ADC but shouldn't prevent the user building their circuit to use the most resolution.

DAC LIMITING/OTHER SAFETY FEATURES

Limit registers (called DPLIMn and DNLIMn) on the device offer the user some protection from firmware bugs which could cause catastrophic board problems by forcing supplies beyond their allowable output ranges. Essentially the DAC code written into the DACn register is clipped such that the code used to set the DAC voltage is actually given by

```
DAC Code
= DACn, DACn ≥ DNLIMn and DACn ≤ DPLIMn
= DNLIMn,      DACn < DNLIMn
= DPLIMn,      DACn > DPLIMn
```

In addition, the DAC output buffer is tri-stated if DNLIMn > DPLIMn. In this way it is possible for the user to make it very difficult for the DAC output buffers to be turned on at all in normal system operation by programming the limit registers in this way (these are among the registers downloaded from EEPROM at startup).

COMMUNICATING WITH THE ADM1066

CONFIGURATION DOWNLOAD AT POWER-UP

The configuration of the ADM1066– the UV/OV thresholds, glitch filter timeouts, PDO configurations etc, is dictated by the contents of RAM. The RAM is comprised of digital latches which are local to each of the functions on the device. The latches are "double buffered" and actually comprised of two identical latches, Latch A and Latch B. Thus, the update of a function first updates the contents of Latch A and then updates the contents of Latch B with identical data. The advantage of the architecture is explained in detail below. These latches are volatile memory and lose their contents at power- down. Therefore, at power- up the configuration in the RAM must be restored. This is achieved by downloading the contents of the EEPROM (non- volatile memory) to the local latches. This download occurs in a number of steps.

1. With no power applied to the device, the PDO's are all high impedance.
2. Once 1V appears on any of the inputs connected to the VDD Arbitrator (VH or VPn), the PDO's are all weakly pulled to GND with a 20kΩ impedance.
3. Once the supply rises above the Under voltage Lockout of the device (UVLO is 2.5V), the EEPROM starts to download to the RAM.
4. The EEPROM downloads its contents to all Latch A's.
5. Once the contents of the EEPROM are completely downloaded to Latch A's, the device controller signals all Latch A's to download to all Latch B's simultaneously, thus completing the configuration download.
6. 0.5ms after the configuration download, the first state definition is downloaded from EEPROM into the Sequencing Engine

Note– Any attempt to communicate with the device prior to this download completion will result in a NACK being issued from the ADM1066.

UPDATING THE CONFIGURATION OF THE ADM1066

Once powered up, with all of the configuration settings loaded from EEPROM into the RAM registers, the user may wish to alter the configuration of functions on the ADM1066 (eg) change the UV or OV limit of an SFD, change the fault output of an SFD, change the rise time delay of one of the PDO's etc.

The ADM1066 provides a number of options which allow the user to update the configuration differently over the SMBus interface. All of these options are controlled in the register UPDCFG. The options are:

1. Update the configuration in real time. The user writes to RAM across the SMBus and the configuration is updated immediately.
2. Update A Latches without updating the B Latches. With this method, the configuration of the ADM1066 will remain unchanged and continue to operate in the original setup until the instruction is given to update the B Latches.
3. Change EEPROM register contents without changing the RAM contents, and then download the revised EEPROM contents to the RAM registers. Again, with this method, the configuration of the ADM1066 will remain unchanged and continue to operate in the original setup until the instruction is given to update the RAM.

The instruction to download from the EEPROM in option 3 above is also a useful way to restore the original EEPROM contents if revisions to the configuration are unsatisfactory. If the user alters, say, an OV threshold they can do this by updating the RAM register as described in 1 above. If they are not satisfied with this change and wish to revert to the original programmed value, then the device controller can issue a command to download the EEPROM contents to the RAM again, thus restoring the ADM1066 to its original configuration.

This type of operation is possible because of the topology of the ADM1066. The Local (volatile) registers, or RAM, are all double buffered latches. Setting bit 0 of the UPDCFG register to 1 leaves the double buffered latches open at all times. If bit 0 is set to 0, then when RAM write occurs across the SMBus only the first side of the double buffered latch is written to. The user must then write a 1 to bit 1 of the UPDCFG register. This generates a pulse to update all of the second latches at once. Similarly with EEPROM writes.

A final bit in this register is used to enable EEPROM page erasure. If this bit is set high, then the contents of an EEPROM page can all be set to 1. If low, then the contents of a page cannot be erased, even if the command code for page erasure is programmed across the SMBus. The bitmap for register UPDCFG is shown in AN-698. A flow chart for download at power up and subsequent configuration updates is shown in Figure 35 overleaf.

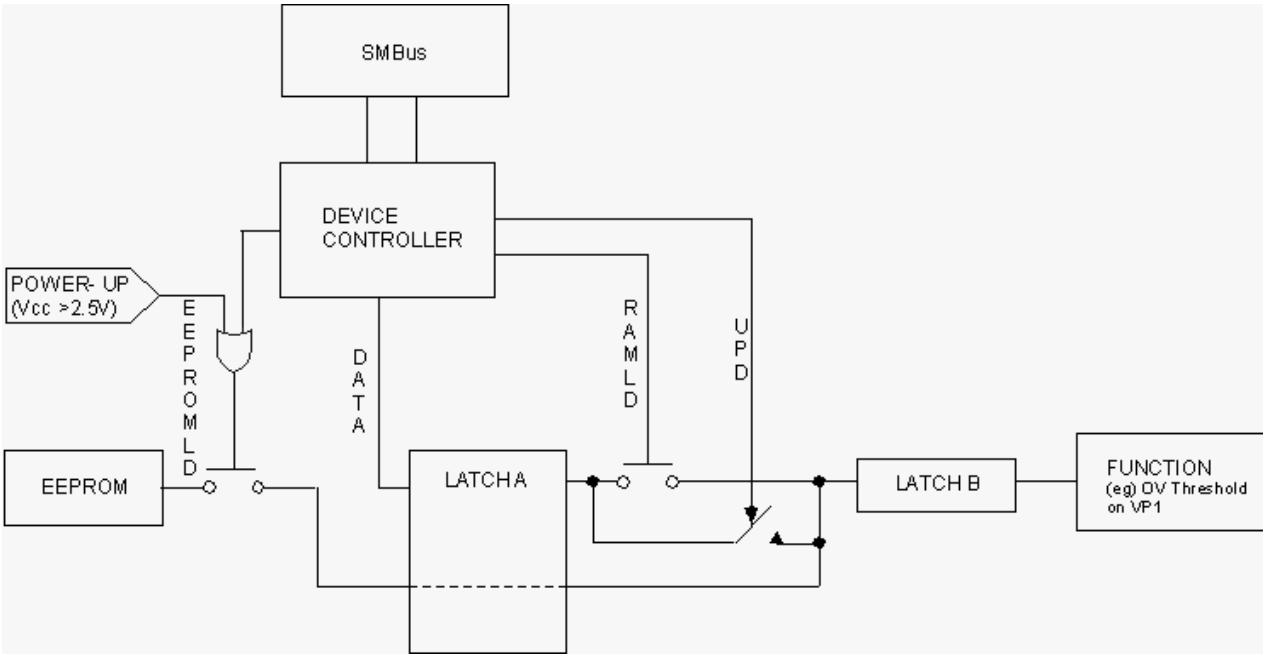

Figure 35. Configuration Update Flow Diagram

UPDATING THE SEQUENCING ENGINE OF THE ADM1066

The update of the SE functions differently to the regular configuration latches. The SE has its own dedicated 512 byte EEPROM for storing State definitions, providing 63 individual states with a 64- bit word each (one state is reserved). At power-up, the first state is loaded from the SE EEPROM into the engine itself. When the conditions of this state are met, the next state is loaded from EEPROM into the engine, and so on. The loading of each new state takes approximately 20µs. If a state is to be altered, then the required changes must be made directly to EEPROM. RAM for each state does not exist. The relevant alterations must be made to the 64- bit word, which is then uploaded directly to EEPROM.

INTERNAL REGISTERS OF THE ADM1066

The ADM1066 contains a large number of data registers. A brief description of the principal registers is given below.

Address Pointer Register: This register contains the address that selects one of the other internal registers. When writing to the ADM1066, the first byte of data is always a register address, which is written to the Address Pointer Register.

Configuration Registers: Provide control and configuration for various operating parameters of the ADM1066.

ADM1066 EEPROM

The ADM1066 has two 512 byte cells of non-volatile, Electrically-Erasable Programmable Read-Only Memory (EEPROM), from register addresses F800h to FBFFh. This may be used for permanent storage of data that will not be lost when the ADM1066 is powered down, one EEPROM cell containing the configuration data of the device, the other containing the State definitions for the Sequencing Engine. Although referred to as Read Only Memory, the EEPROM can be written to (as well as read from) via the serial bus in exactly the same way as the other registers. The only major differences between the E^2PROM and other registers are:

1. An EEPROM location must be blank before it can be written to. If it contains data, it must first be erased.
2. Writing to EEPROM is slower than writing to RAM.
3. Writing to the EEPROM should be restricted because it has a limited write/cycle life of typically 10,000 write operations, due to the usual EEPROM wear-out mechanisms.

The first EEPROM is split into 16 (0 to 15) pages of 32 Bytes each. Pages 0 to 6, starting at address F800, hold the configuration data for the applications on the ADM1066 (the SFD's, PDO's etc.). These EEPROM addresses are the same as the RAM register addresses, prefixed by F8. Page 7 is reserved. Pages 8 to 15 are for customer use. Data can be downloaded from EEPROM to RAM in one of two ways:–

1. At Power- up, pages 0 to 6 are downloaded.
2. Setting bit 0 of the UDOWNLD Register (D8h) performs a user download of pages 0 to 6.

SERIAL BUS INTERFACE

Control of the ADM1066 is carried out via the serial System Management Bus (SMBus). The ADM1066 is connected to this bus as a slave device, under the control of a master device. It takes approximately 1ms after power up for the ADM1066 to download from it's EEPROM. Therefore access is restricted to the ADM1066 until the download is completed.

IDENTIFYING THE ADM1066 ON THE SMBUS

The ADM1060 has a 7-bit serial bus slave address. When the device is powered up, it will do so with a default serial bus address. The five MSB's of the address are set to 01101, the two LSB's are determined by the logical states of pin A1 and A0. This allows the connection of 4 ADM1066's to the one SMBus. The device also has a number of identification registers (read only) which can be read across the SMBus. Table 7 lists these registers, their values, and functions.

Table 7.

Name Address	Value	Function
MANID F4h	41h	Manufacturer ID for Analog Devices
REVID F5h	--h	Silicon Revision
MARK1 F6h	--h	S/w brand
MARK2 F7h	--h	S/w brand

GENERAL SMBUS TIMING

Figure 36, Figure 37 and Figure 38 show timing diagrams for general read and write operations using the SMBus. The SMBus specification defines specific conditions for different types of read and write operation, which are discussed later.

The general SMBus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA whilst the serial clock line SCL remains high. This indicates that a data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit slave address (MSB first) plus a R/$\overline{W}$ bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device (0 = write, 1 = read).

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit, and holding it low during the high period of this clock pulse. All other devices on the bus now remain idle whilst the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0 then the master will write to the slave device. If the R/$\overline{W}$ bit is a 1 the master will read from the slave device.

2. Data is sent over the serial bus in sequences of 9 clock pulses, 8 bits of data followed by an Acknowledge Bit from the slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal. If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction such as telling the slave device to expect a block write, or it may simply be a register address that tells the slave where subsequent data is to be written. Since data can flow in only one direction as defined by the R/$\overline{W}$ bit, it is not possible to send a command to a slave device during a read operation. Before doing a read operation, it may first be necessary to do a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will release the SDA line during the low period before the 9th clock pulse, but the slave device will not pull it low. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition

SMBUS PROTOCOLS FOR RAM AND EEPROM

The ADM1066 contains volatile registers (RAM) and non-volatile EEPROM. User RAM occupies address locations from 00h to DFh, whilst EEPROM occupies addresses from F800h to FBFFh.

Data can be written to and read from both RAM and EEPROM as single data bytes.

Data can only be written to unprogrammed EEPROM locations. To write new data to a programmed location it is first necessary to erase it. EEPROM erasure cannot be done at the byte level, the EEPROM is arranged as 32 pages of 32 bytes, and an entire page must be erased.

Page erasure is enabled by setting bit 2 in register UPDCFG (address 90h) to 1. If this is not set then page erasure cannot occur, even if the command byte (FEh) is programmed across the SMBus.

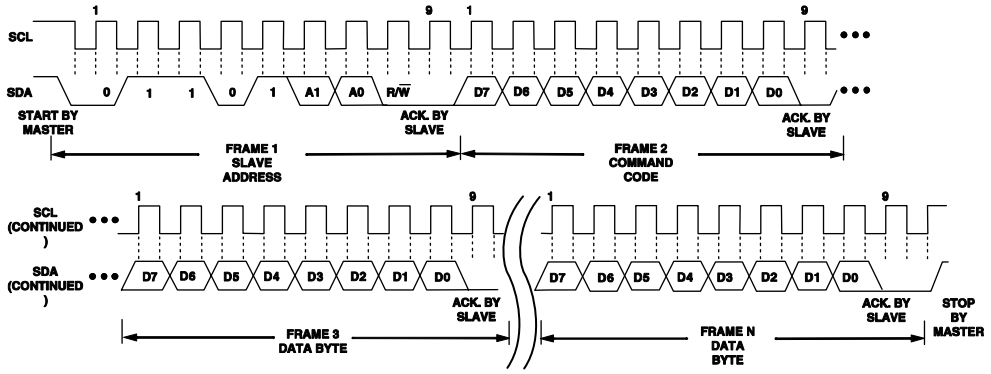

Figure 36. General SMBus Write Timing Diagram

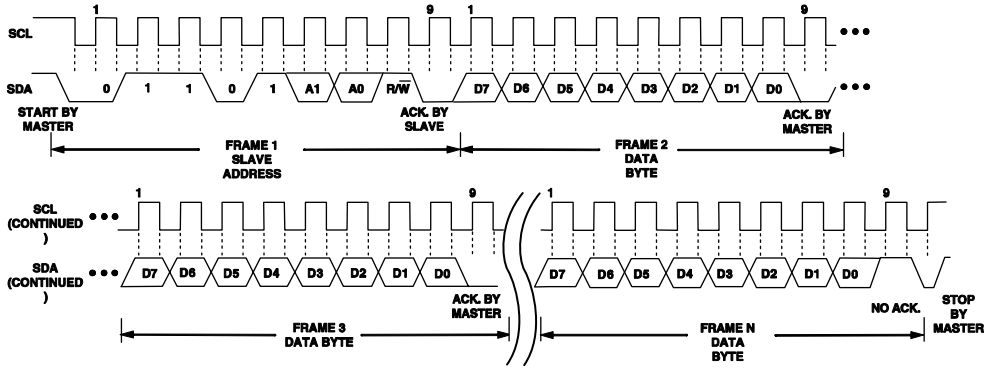

Figure 37. General SMBus Read Timing Diagram

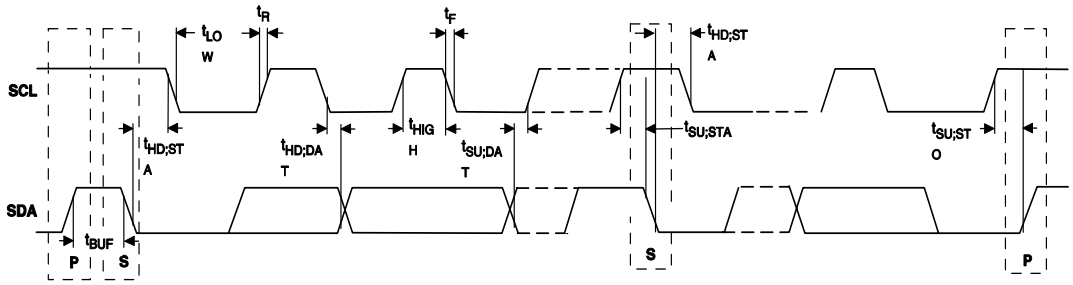

Figure 38. Diagram for Serial Bus Timing

ADM1066 WRITE OPERATIONS

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADM1066 are discussed below. The following abbreviations are used in the diagrams:

S – START

P – STOP

R – READ

W – WRITE

A – ACKNOWLEDGE

$\overline{A}$ – NO ACKNOWLEDGE

The ADM1066 uses the following SMBus write protocols:

Send Byte

In this operation the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a STOP condition on SDA and the transaction ends.

In the ADM1066, the send byte protocol is used for two purposes.

1. To write a register address to RAM for a subsequent single byte read from the same address or block read or write starting at that address. This is illustrated in Figure *39*.

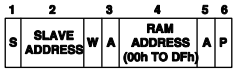

Figure 39. Setting A RAM Address For Subsequent Read

2. Erase a page of EEPROM memory. EEPROM memory can be written to only if it is unprogrammed. Before writing to one or more EEPROM memory locations that are already programmed, the page or pages containing those locations must first be erased. EEPROM memory is erased by writing a command byte.

   The master sends a command code that tells the slave device to erase the page. The ADM1066 command code for a pages(s) erasure is FEh (11111110). Note that, in order for page erasure to take place, the page address has to be given in the previous write word transaction (see write byte below). Also, bit 2 in register UPDCFG (address 90h) must be set to 1.

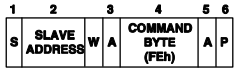

Figure 40. EEPROM Page Erasure

   As soon as the ADM1066 receives the command byte, page erasure begins. The master device can send a STOP command as soon as it sends the command byte. Page erasure takes approximately 20ms. If the ADM1066 is accessed before erasure is complete, it will respond with a NACK.

Write Byte/Word

In this operation the master device sends a command byte and one or two data bytes to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master sends a data byte (or may assert STOP at this point).
9. The slave asserts ACK on SDA.
10. The master asserts a STOP condition on SDA to end the transaction.

In the ADM1066, the write byte/word protocol is used for three purposes.

1. Write a single byte of data to RAM. In this case the command byte is the RAM address from 00h to DFh and the (only) data byte is the actual data. This is illustrated in Figure 41

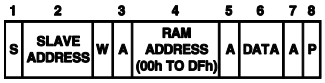

Figure 41. Single Byte Write To RAM

2. Set up a two byte EEPROM address for a subsequent read, write, block read, block write or page erase. In this case the command byte is the high byte of the EEPROM address

from F8h to FBh. The (only) data byte is the low byte of the EEPROM address. This is illustrated in Figure 42.

Figure 42. Setting An EEPROM Address

Note for page erasure that as a page consists of 32 bytes only the three MSB's of the address low byte are important. The lower 5 bits of the EEPROM address low byte only specify addresses within a page and are ignored during an erase operation.

3. Write a single byte of data to EEPROM. In this case the command byte is the high byte of the EEPROM address from F8h to FBh. The first data byte is the low byte of the EEPROM address and the second data byte is the actual data. This is illustrated in Figure 43

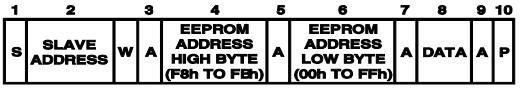

Figure 43. Single Byte Write To EEPROM

Block Write

In this operation the master device writes a block of data to a slave device. The start address for a block write must previously have been set. In the case of the ADM1066 this is done by a Send Byte operation to set a RAM address or a Write Byte/Word operation to set an EEPROM address.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code that tells the slave device to expect a block write. The ADM1066 command code for a block write is FCh (11111100).
5. The slave asserts ACK on SDA.
6. The master sends a data byte that tells the slave device how many data bytes will be sent. The SMBus specification allows a maximum of 32 data bytes to be sent in a block write.
7. The slave asserts ACK on SDA.
8. The master sends N data bytes.
9. The slave asserts ACK on SDA after each data byte.
10. The master asserts a STOP condition on SDA to end the transaction.

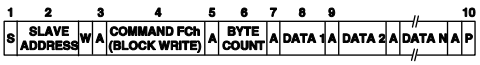

Figure 44. Block Write To EEPROM Or RAM

Unlike some EEPROM devices which limit block writes to within a page boundary, there is no limitation on the start address when performing a block write to EEPROM, except:

1. There must be at least N locations from the start address to the highest EEPROM address (FBFFh), to avoiding writing to invalid addresses.
2. If the addresses cross a page boundary, both pages must be erased before programming.

Note that the ADM1066 features a clock extend function for writes to EEPROM. Programming an EEPROM byte takes approximately 250µs, which would limit the SMBus clock for repeated or block write operations. The ADM1066 pulls SCL low and extends the clock pulse when it cannot accept any more data.

ADM1066 READ OPERATIONS

The ADM1066 uses the following SMBus read protocols:

Receive Byte

In this operation the master device receives a single byte from a slave device, as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a STOP condition on SDA and the transaction ends.

In the ADM1066, the receive byte protocol is used to read a single byte of data from a RAM or EEPROM location whose address has previously been set by a send byte or write byte/word operation. This is illustrated in Figure 45.

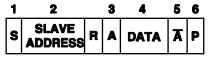

Figure 45. Single Byte Read From EEPROM Or RAM

Block Read

In this operation the master device reads a block of data from a slave device. The start address for a block read must previously have been set. In the case of the ADM1066 this is done by a Send Byte operation to set a RAM address, or a Write Byte/Word operation to set an EEPROM address. The block read operation itself consists of a Send Byte operation that sends a block read command to the slave, immediately followed by a repeated start and a read operation that reads out multiple data bytes, as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code that tells the slave device to expect a block read. The ADM1066 command code for a block read is FDh (11111101).
5. The slave asserts ACK on SDA.
6. The master asserts a repeat start condition on SDA.
7. The master sends the 7-bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The ADM1066 sends a byte count data byte that tells the master how many data bytes to expect. The ADM1066 will always return 32 data bytes (20h), which is the maximum allowed by the SMBus 1.1 specification.
10. The master asserts ACK on SDA.
11. The master receives 32 data bytes.
12. The master asserts ACK on SDA after each data byte.
13. The master asserts a STOP condition on SDA to end the transaction.

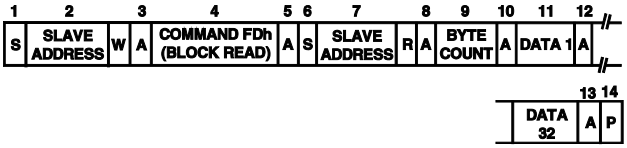

Figure 46. Block Read From EEPROM or RAM

Error Correction

The ADM1066 provides the option of issuing a PEC (Packet Error Correction) byte after a write to RAM, a write to EEPROM, a block write to RAM/EEPROM or a block read from RAM/EEPROM. This enables the user to verify that the data received by or sent from the ADM1066 is correct. The PEC byte is an optional byte sent after that last data byte has been written to or read from the ADM1066. The protocol is as follows:–

1. The ADM1066 issues a PEC byte to the master. The master should check the PEC byte and issue another block read if the PEC byte is incorrect.
2. A NACK is generated after the PEC byte to signal the end of the read.

Note: The PEC byte is calculated using CRC-8. The Frame Check Sequence (FCS) conforms to CRC-8 by the polynomial:–

$$C(x) = x^8 + x^2 + x^1 + 1$$

Consult SMBus 1.1 specification for more information. An example of a block read with the optional PEC byte is shown in Figure 47 below.

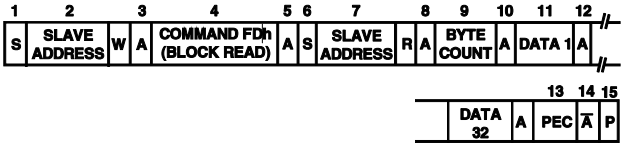

Figure 47. Block Read From EEPROM or RAM with PEC

OUTLINE DIMENSIONS

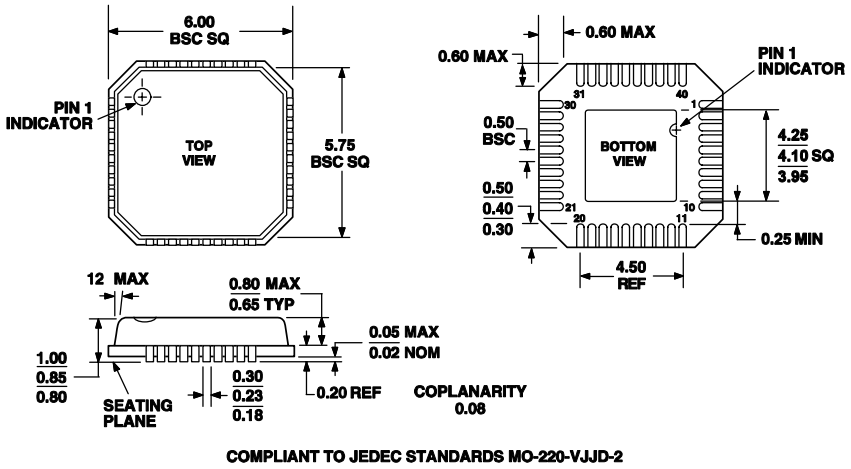

Figure 48. 40-Lead 6×6 Chip Scale Package (CP-40)
Dimensions shown in millimeters

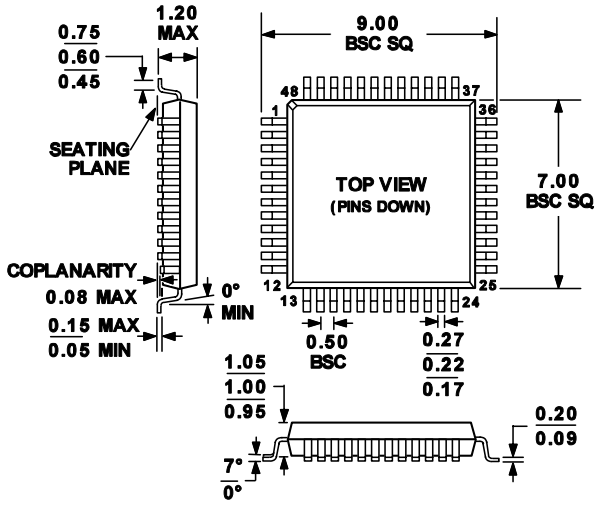

Figure 49. 48-Lead 7×7 TQFP Package (SU-48)
Dimensions shown in millimeters

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Model	Temperature Range	Package Description	Package Option
ADM1066ACP-U3	−40°C to +85°C	40-Lead LFCSP	CP-40
ADM1066ASU-U3	−40°C to +85°C	48-Lead TQFP	SU-48

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